AF
JFW

OIPE IAP38
OCT 24 2005
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR:	Zhong-Ning (George) CAI
SERIAL NO:	09/749,792
FILING DATE:	December 28, 2000
TITLE:	METHOD AND APPARATUS FOR THERMAL SENSITIVITY BASED ON DYNAMIC POWER CONTROL
ART UNIT:	2116
EXAMINER:	Tse W. CHEN

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

SIR:

This is a brief in support of an appeal filed in the above-identified application.

I. Real Party in Interest

The real party in interest is the Assignee, Intel Corporation.

II. Related Appeals and Interferences

There are no other appeals or interferences known to Appellant, Appellant's legal representative, or Assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in this Appeal.

III. Status of Claims

Claims 1-17 were originally filed in the application on December 28, 2000. Claims 18-20 were added in an amendment filed September 13, 2004. No claims were canceled. Claims 1-20 are finally rejected and on appeal.

IV. Status of Amendments

No amendments were filed subsequent to final rejection.

V. Summary of Claimed Subject Matter

Independent claim 1.

An apparatus for dynamic power control of a processor based on a thermal condition, comprising:

a sensor to measure a thermal characteristic of a processor with a clock frequency;

a circuit to reduce the clock frequency of the processor responsive to the measured thermal characteristic satisfying a pre-determined threshold, the circuit including a performance demanding level input to determine a rate of the temperature-related frequency reduction .

Explanation.

Embodiments of the present invention relate to thermal throttling in processors. The embodiments may include a thermal sensor to measure temperature of a processor die (page 5, line 2; FIG. 3, thermal sensor 335). The thermal sensor may be coupled to a circuit for frequency reduction in response to temperature (page 5, lines 2-3; FIG. 3, frequency reduction circuit 305). This reduction in frequency may result in a corresponding cooling of the processor, thereby avoiding malfunctions that can occur at high temperatures (page 1, lines 25-26).

The frequency reduction circuit may reduce a clock frequency of the processor responsive to a measured thermal characteristic satisfying a pre-

determined threshold (page 5, lines 15-17). When the threshold is met or exceeded, the frequency reduction circuit may assert an enabling signal which removes switching transitions from the clock signal to lower its frequency (page 8, lines 13-17; FIG. 3, enabling signal 311, clock signal 330).

The frequency reduction circuit may include a performance demanding level (PDL) input (page 5, line 14; FIG. 3, performance demanding level input 311). The PDL may determine a rate of temperature-related frequency reduction of the processor clock. For example, if the PDL signal is asserted, frequency reduction may be non-aggressive, e.g., only a 1/5 reduction from normal clock frequency (page 7, lines10-12). On the other hand, if the PDL signal is not asserted, frequency reduction may be aggressive, e.g., close to a 50% reduction from normal clock frequency (page 7, lines13-15). The PDL signal enables frequency reduction that is, for example, responsive to the execution of particular applications depending on their requirements for processor speed (page 7, lines 16-24 to page 8, lines 1-2).

Independent claim 7.

A method for dynamic power control of a processor based on a thermal condition, comprising:

measuring a thermal characteristic of a processor with a clock frequency;

reducing the clock frequency in response to the measured thermal characteristic satisfying a pre-determined threshold, and in accordance with a performance demanding level input value that determines a rate of the temperature-related frequency reduction.

Explanation.

Independent claim 7 is a method claim substantially paralleling claim 1, explained previously.

Independent claim 12.

A method for using control logic to provide dynamic power control of a processor based on a thermal condition, comprising:

entering a first state from a second state in response to a measured thermal characteristic of a processor with a clock frequency failing to satisfy a first pre-determined threshold where the first state outputs the clock frequency for the processor and the second state reduces the clock frequency for the processor;

remaining in the first state in response to a measured thermal characteristic of the processor failing to satisfy the first pre-determined threshold; and

entering the second state from the first state in response to a measured thermal characteristic of the processor satisfying the first pre-determined threshold, and in the second state, performing frequency reduction in accordance with a performance demanding level input value that determines a rate of the temperature-related frequency reduction.

Explanation.

Embodiments of the invention further relate to a plurality of states depending on a measured thermal characteristic of a processor (page 10, lines 14-21; FIGs. 5 and 6). The states include a wait state in which clock frequency is normal, and an active state in which frequency reduction is performed (FIGs. 5 and 6; page 11, lines 21-24; page 11, lines 11-12). A transition from the active state to the wait state may occur when a thermal characteristic does not satisfy a predetermined threshold (page 13, lines 1-4; FIGs. 5 and 6).

The wait state may continue while the thermal characteristic remains below the threshold (page 13, lines 1-4; FIGs. 5 and 6). However, when the threshold is met or exceeded, a transition from the wait state to the active state may occur (page 12, lines 3-6; FIGs. 5 and 6). In the active state, frequency

reduction may occur in accordance with a PDL input as described with reference to claim 1.

Independent claim 18.

A processor comprising:

thermal sensing logic to output function signals taking on values representing a function of a temperature and a rate of temperature change, and an enabling signal taking on values responsive to whether the function signals meet or do not meet predetermined temperature and rate of temperature change thresholds;

performance demanding level logic to output a signal taking on values that respectively permit a first rate of temperature-related frequency reduction and a second rate of temperature-related frequency reduction, the first rate of frequency reduction being higher than the second; and

frequency reduction logic coupled to the performance demanding level logic and the thermal sensing logic, to perform frequency reduction based on the values generated by the thermal sensing logic and the performance demanding level logic.

Explanation.

Claim 18 is a processor claim whose recitations substantially parallel those of claim 1, explained previously.

VI. Grounds of Rejection to be Reviewed on Appeal

A. Claims 1-4, 6-9 and 11-17 are rejected under 35 USC 103(a) as being unpatentable over Georgiou et al. (US 5,940,785), in view of McDermott (US 5,233,314).

B. Claims 5 and 10 are rejected under 35 USC 103(a) as being unpatentable over Georgiou et al. and McDermott in view of Ko (US 6,192,479).

C. Claims 18-20 are rejected under 35 USC 103(a) as being unpatentable over Ko in view of Georgiou and McDermott.

VII. Argument

A. Claims 1-4, 6-9 and 11-17 are allowable over Georgiou et al. and McDermott.

Georgiou et al. and McDermott do not suggest a performance demanding level input to determine a rate of temperature-related frequency reduction, as recited in each of independent claims 1, 7 and 12.

As discussed above, embodiments of the present invention relate to a frequency reduction circuit that includes a performance demanding level (PDL) input to determine a rate of temperature-related frequency reduction. Among other things, the PDL signal lets the frequency reduction circuit be sensitive to particular applications. For example, during a period of frequency reduction in response to high temperatures, if a hardware component (e.g. a hard drive) is running an application that does not require great processor speed, aggressive frequency reduction may be performed, by not asserting the PDL signal. On the other hand, if a hardware component requires high processor speed, frequency reduction with finer granularity may be performed by asserting the PDL signal.

Georgiou et al. (hereafter, "Georgiou") and McDermott suggest nothing resembling the claimed PDL input feature. The Examiner recognizes this with respect to Georgiou (final Office Action mailed 3/21/05 (hereafter, "Office Action"), page 3, item 6). However, the Examiner alleges that McDermott remedies this deficiency in McDermott. The Examiner cites to McDermott at col. 4, lines 66 to col. 5, line 24, col. 6, lines 51-64, and col. 8, line 45 to col. 9, line 13

as disclosing "a performance demanding level input [lvl1, 2] to determine a rate of the frequency reduction" (Office Action, page 3, item 7). The Examiner further contends:

> "It would have been obvious to one of ordinary skill in the art, having the teachings of Georgiou and McDermott before him at the time the invention was made, to modify ***the circuit that includes an input to determine a temperature-related frequency reduction*** as taught by Georgiou to include the teachings regarding ***controlling frequency reductions via a rate*** as taught by McDermott, in order to obtain [the PDL input of the rejected claims]."

(Office Action, item 8; emphasis in original.) As motivation for the combination of Georgiou with McDermott, the Examiner offers the view that the combination "provides a way to better control frequency changes," and cites McDermott at col. 2, line 65 to col. 3, line 23 (Office Action, item 8).

The Examiner's position is in error. The LVL1, LVL2 signals cited by the Examiner are in no way involved in frequency reduction based on temperature. Instead, the LVL1, LVL2 signals are part of a phase-locked loop (PLL) circuit, and relate to synchronization of the PLL circuit. The PLL circuit has a phase comparator that outputs control signals FUP, FDN, LVL1 and LVL2. See McDermott, FIG. 2, and col. 5, lines 13-24. The FUP, FDN signals are to increase or decrease, respectively, the output frequency of a voltage controlled oscillator responsive to a phase relationship between an input clock and a feedback signal. The LVL1, LVL2 signals control the rate of increase or decrease based on a difference between the input clock and the feedback signal. See McDermott, FIG. 2 and col. 5, lines 21-24.

Portions of McDermott reproduced below clearly indicate that the LVL1, LVL2 signals have nothing to do with temperature-related control of frequency:

> "For purposes of this example, line FUP indicates that the frequency of the output clock signal is to increase, line FDN indicates that the frequency of the output

clock signal is to decrease, and lines LVL2, LVL 1 control the rate of change of the frequency *according to the degree to which the input and reference clock signals are synchronized with one another.*"

(Col. 5, lines 17-24; emphasis added.)

"Phase comparator 14 according to the preferred embodiment of the invention further includes circuitry for presenting level signals to current source 16 on lines LVL2, LVL1 corresponding to the number of pump-up/pump-down cycles generated by phase comparator 14, and thus *the number of overshoot/undershoot cycles of the output clock signal frequency relative to the input clock frequency.* These level signals on line LVL2, LVL1 reduce the rate at which VCO 20 is to change its output frequency with the occurrence of pump-up/pump-down cycles. As a result, according to the present invention, the output clock frequency converges to the input clock frequency with each pump-up/pump-down cycle."

(Col. 6, lines 51 -61; emphasis added.) In view of the above, the LVL1 and LVL2 signals in McDermott clearly relate only to the synchronization of a PLL. Thus, at most the combination of Georgiou with McDermott yields Georgiou's device plus an improved PLL. The performance demanding level input to determine a rate of temperature-related frequency reduction, called for independent claims 1, 7 and 12, is totally absent from the combination of Georgiou and McDermott.

Further, no credible motivation for the modification to Georgiou proposed by the Examiner is provided. To the contrary, the portion of McDermott cited by the Examiner as motivating the combination with Georgiou (col. 2, line 65 to col. 3, line 23) bears out the inappositeness of McDermott as a reference. Here, McDermott states the various "objects of the ... invention," e.g., "to provide a fully-integrated charge pump PLL having a fast response time to input frequency

changes as well as highly stable behavior in the phase-locked condition" (col. 2, lines 65-68), "to provide ... a circuit which has selectably variable response times in the loop filter" (col. 3, lines 1-3), and "to provide such a circuit in which the slew rate of the loop filter is controlled according to the relationship between the input and feedback clock signals" (col. 3, lines 4-7). These objects do not motivate modification of a thermal throttling system for processors; rather, they motivate improvements to a PLL.

Indeed, the combination of Georgiou and McDermott to reject the present claims is itself error. "[I]n order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPW2d 1443, 1445 (Fed. Cir. 1992). McDermott fails this test. As discussed, McDermott is concerned with synchronization of a PLL, while the rejected claims relate to temperature-related frequency reduction.

The Examiner, as noted above, in fact states in the final Office Action that McDermott is only cited as teaching controlling a rate of frequency reduction. The Advisory Action mailed September 9, 2005 has more along these lines. Here, the Examiner observes that "McDermott was cited to teach a rate of reduction controlled by the LVL1, LVL2 signals representing a performance demanding level in the broadest interpretation, i.e., as in how fast or slow should the rate of reduction be." No connection is drawn between the field of PLL design as in McDermott, and thermal throttling as in the rejected claims. Clearly the broad interpretation applied by the Examiner did not yield, in McDermott, prior art suitable as a reference to reject the claims on appeal.

Independent claims 1, 7 and 12 are therefore allowable over Georgiou and McDermott. Claims 2-4, 6, 8, 9, 11 and 13-17 are likewise allowable over Georgiou and McDermott for at least the reason that they include the recitations of one of claims 1, 7 and 12 by dependence thereon.

B. Claims 5 and 10 are allowable over Georgiou and McDermott in view of Ko.

Claims 5 and 10 were rejected under 35 USC 103(a) as being unpatentable over Georgiou and McDermott as applied to claims 1 and 7, and further in view of Ko. Claims 5 and 10 depend on independent claims 1 and 7, respectively. Accordingly, claims 5 and 10 are allowable over Georgiou and McDermott for at least the reason that they include the recitations of these respective independent claims. Ko does not cure the deficiencies in Georgiou and McDermott with respect to the independent claims. For example, the Examiner recognizes that Ko does not disclose a performance demanding level input to determine a rate of temperature-related frequency reduction, as recited in each of independent claims 1, 7 and 12 (Office Action, page 6, item 22). Thus, claims 5 and 10 are similarly allowable over the combination of Georgiou, McDermott and Ko.

C. Claims 18-20 are allowable over Ko in view of Georgiou and McDermott.

Claims 18-20 were rejected under 35 USC 103(a) as being unpatentable over Ko in view of Georgiou and McDermott. Along lines discussed above, Ko, Georgiou and McDermott are silent with regard to a performance demanding level input as recited in independent claim 18, and as included in claims 19 and 20 by dependence on claim 18.

Conclusion

In view of the above, it is clear that the Examiner erred in finally rejecting claims 1-20. It is therefore respectfully requested that the Board reverse the Examiner and allow claims1-20.

The Examiner is invited to contact the undersigned at (202) 220-4323 to discuss any matter concerning this application. The Office is authorized to charge any fees related to this communication to Deposit Account No. 11-0600.

Respectfully submitted,

Dated: 10/24/01

By: _____
William E. Curry
Reg. No. 43,572

KENYON & KENYON
Attorneys for Intel Corporation
1500 K Street, N.W., Suite 700
Washington, D.C. 20005
Tel: (202) 220-4200
Fax:(202) 220-4201

CLAIMS APPENDIX

1. An apparatus for dynamic power control of a processor based on a thermal condition, comprising:

a sensor to measure a thermal characteristic of a processor with a clock frequency;

a circuit to reduce the clock frequency of the processor responsive to the measured thermal characteristic satisfying a pre-determined threshold, the circuit including a performance demanding level input to determine a rate of the temperature-related frequency reduction .

2. The apparatus of claim 1, wherein the thermal characteristic includes temperature and rate of temperature change.

3. The apparatus of claim 1, wherein the circuit includes a frequency generator and a logic circuit.

4. The apparatus of claim 1, wherein the circuit reduces the clock frequency by less than fifty percent.

5. The apparatus of claim 1, wherein the circuit reduces the clock frequency by removing a pre-determined number of transitions from a signal producing the clock frequency.

6. The apparatus of claim 1, wherein the sensor and circuit produce a higher operating temperature for the processor.

7. A method for dynamic power control of a processor based on a thermal

condition, comprising:

measuring a thermal characteristic of a processor with a clock frequency;

reducing the clock frequency in response to the measured thermal characteristic satisfying a pre-determined threshold, and in accordance with a performance demanding level input value that determines a rate of the temperature-related frequency reduction.

8. The method of claim 7, wherein the step of measuring includes measuring temperature and rate of temperature change.

9. The method of claim 7, wherein the step of reducing includes reducing the clock frequency by less than fifty percent.

10. The method of claim 7, wherein the step of reducing includes reducing the clock frequency by removing a pre-determined number of transitions from a signal producing the clock frequency.

11. The method of claim 10, wherein the step of reducing includes reducing the clock frequency in response to the measured thermal characteristic satisfying a pre-determined threshold to produce a higher operating temperature of the processor.

12. A method for using control logic to provide dynamic power control of a processor based on a thermal condition, comprising:

entering a first state from a second state in response to a measured thermal characteristic of a processor with a clock frequency failing to satisfy a first pre-determined threshold where the first state outputs the clock frequency for the processor and the second state reduces the clock frequency for the processor;

remaining in the first state in response to a measured thermal characteristic of the processor failing to satisfy the first pre-determined threshold; and

entering the second state from the first state in response to a measured thermal characteristic of the processor satisfying the first pre-determined threshold, and in the second state, performing frequency reduction in accordance with a performance demanding level input value that determines a rate of the temperature-related frequency reduction.

13. The method of claim 12, wherein the thermal characteristic of the processor includes temperature and rate of temperature change.

14. The method of claim 12, further comprising:

entering a third state from the first state in response to a measured thermal characteristic of the processor satisfying a second pre-determined threshold where the third state waits for a measured thermal characteristic of the processor to satisfy a third pre-determined threshold to reduce the clock frequency for the processor;

remaining in the third state in response to a measured thermal characteristic of the processor failing to satisfy the third pre-determined threshold; and

entering the first state from the third state in response to a measured thermal characteristic failing to satisfy the second pre-determined threshold.

15. The method of claim 14, wherein the second pre-determined threshold is a temperature threshold, and the third pre-determined threshold is a rate of temperature change threshold.

16. The method of claim 14, further comprising:

entering the second state from the third state in response to a measured thermal characteristic of the processor satisfying the third pre-determined threshold;

remaining in the second state in response to a measured thermal characteristic of the processor satisfying the third pre-determined threshold; and

entering the third state from the second state in response to a measured thermal characteristic of the processor failing to satisfy the second pre-determined threshold.

17. The method of claim 16, wherein the second pre-determined threshold is a temperature threshold, and the third pre-determined threshold is a rate of temperature change threshold.

18. A processor comprising:

thermal sensing logic to output function signals taking on values representing a function of a temperature and a rate of temperature change, and an enabling signal taking on values responsive to whether the function signals meet or do not meet predetermined temperature and rate of temperature change thresholds;

performance demanding level logic to output a signal taking on values that respectively permit a first rate of temperature-related frequency reduction and a second rate of temperature-related frequency reduction, the first rate of frequency reduction being higher than the second; and

frequency reduction logic coupled to the performance demanding level logic and the thermal sensing logic, to perform frequency reduction based on the values generated by the thermal sensing logic and the performance demanding level logic.

19. The processor of claim 18, wherein the function signals and the enabling signal and associated logic implement a state machine to cyclically enter one of first, second and third states, the first state corresponding to a condition wherein the function signals indicate that the predetermined temperature and rate of temperature change thresholds are not met and therefore frequency reduction is not performed, the third state corresponding to a condition wherein the function signals indicate that the predetermined temperature and rate of temperature change thresholds are met and therefore frequency reduction is performed, and the second state corresponding to a condition wherein one of the predetermined temperature threshold and the predetermined rate of temperature change threshold is met but the other is not, each of the first, second and third states being enterable from the other states.

20. The processor of claim 18, wherein values output by the performance demanding level logic are responsive to a processor application.

EVIDENCE APPENDIX

As of the time of this filing, no evidence has been submitted.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings.